IN THE CLAIMS

1. (Currently amended) An electronic memory test structure for testing a CAM having a memory array containing memory cells, the electronic test structure comprising:

a dummy match row unit coupled to the memory array and configured to match layout parasitics of [[the]] match lines of the memory cells;

a dummy match column having dummy match cells coupled to the memory array through the match lines, said dummy match column being configured so as to match bitline loading of the memory cells during a search;

a dummy timing circuit coupled to the dummy match column and to the dummy match row, said dummy timing circuit being configured to always generate a miss on a dummy match line during the search; and

a dummy match control circuit coupled to the dummy timing circuit.

2. (Original) The electronic memory test structure according to claim 1, wherein the dummy match column is configured so as not to pull the match lines to a logic high state during a normal search mode.

3. (Original) The electronic memory test structure according to claim 1, wherein the dummy match control circuit causes a transition so as to match the timing of bitline transitions of the memory cells.

4. (Original) The electronic memory test structure according to claim 1, wherein the dummy timing circuit always generates a miss on the dummy match line by causing the dummy match line to transit to a high state.

5. (Original) The electronic memory test structure according to claim 1, wherein:

the dummy match control circuit has a low search input and one of a low match state and a high match state; and

mask inputs are set to high so that the memory array is not searched.

6. (Original) The electronic memory test structure according to claim 5, further comprising:

a priority encoder coupled to the memory array through the match lines.

7. (Original) The electronic memory test structure according to

claim 6, further comprising:

a priority encoder control unit coupled to the priority encoder, and to the dummy match row unit through the dummy match line.

8. (Original) The electronic memory test structure according to claim 6, wherein each cell of the dummy match column generates a logic high level on the match lines during a test mode for passing onto the memory array.

9. (Original) The electronic memory test structure according to claim 6, wherein any cell of the dummy match column does not generate a logic high level on the match lines during another test mode.

10. (Original) The electronic memory test structure according to claim 8, wherein the priority encoder receives all the generated logic high levels through the match lines.

11. (Original) The electronic memory test structure according to claim 9, wherein the match lines from the memory array to the priority encoder are at low levels.

12. (Original) The electronic memory test structure according to claim 8, wherein the test mode is all-hits mode.

13. (Original) The electronic memory test structure according to claim 9, wherein the other test mode is all-misses mode.

14. (Original) The electronic memory test structure according to claim 6, further comprising:

a dummy read row unit and a dummy read column unit coupled to the memory array for matching timing characteristics of the wordline signals of the memory array; and

an interconnected match latch unit and wordline driver coupled between the priority encoder and memory array.

15. (Currently amended) An integrated circuit for testing a CAM having a memory array containing memory cells, comprising:

an integrated circuit substrate having a dummy match row unit coupled to the memory array, said dummy match row unit configured to match layout parasitics of [[the]] match lines of the memory cells;

a dummy match column having dummy match cells coupled to the memory array through the match lines, said dummy match column being configured so as to match bitline loading of the memory cells during a search;

a dummy timing circuit coupled to the dummy match column and

to the dummy match row, said dummy timing circuit being configured to always generate a miss on a dummy match line during the search; and

a dummy match control circuit coupled to the dummy timing circuit.

16-22. (Cancelled)